

REMARKS/ARGUMENTS

I. STATUS OF CLAIMS

Claims 1-30 remain in this application Claims 1 and 16 have been amended.

Claim 1-30 remain rejected in the Office Action by the Examiner.

II. CLAIM REJECTIONS – 35 U.S.C. § 132

The Final Office Action objects to the amendment filed on 5/6/2005. Applicant respectfully disagrees on the basis of said objection and refers to the section below regarding 35 U.S.C. § 112. Applicant believes that the rejection is improper given the disclosure in the Specification and that no new matter has been added.

III. CLAIM REJECTIONS – 35 U.S.C. § 112

The Final Office Action rejects Claims 1 and 16 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art to use and/or make the invention.

Applicant respectfully disagrees. The Examiner states that he has reviewed the specification and could not find support for the limitation of “assigning a virtual IP address to a scheduler”. However, this statement is incorrect. From the Examiner’s statement, it appears that the Examiner searched through the OCR document for the term “virtual IP address”, but the text clearly defines that a virtual IP address is referred to as a “VIP”. The Examiner has ignored Applicant’s explanation and has maintained the

rejection. Therefore, Applicant has extracted further text from the Specification that the Examiner had overlooked which are cited below.

Page 7, lines 4-6 cite that a virtual IP address is defined as a “VIP” throughout the disclosure (emphasis added):

“The first item is supported by all local load balancers. All load balancers publish a **Virtual IP (VIP) address** to the world and then have many machines which can take traffic for that IP address.”

The Specification then further describes the assigning of a VIP to a scheduler in the DLBA on page 11, line 5-page 12, line 11:

“DLBA Scheduler Architecture

All traffic into the array comes in through a box known as the DLBA scheduler. The DLBA scheduler is a DLBA server that has ARPed for the VIP address.

With respect to Fig. 2, all DLBA servers 202, 203, 204 in the array 205 have the VIP address assigned on a loopback interface (or Ethernet alias if possible), but only one machine in the cluster 205 ARPs for the VIP, causing the switch 201 to send all traffic for the VIP to that machine. All machines have the VIP address on an interface (loopback or physical) so they can send traffic back out to the client from the VIP address and so they can take over as the scheduler in case of a scheduler failure. Any machine in the cluster 205 has the ability to become a scheduler at any time in case the current scheduler fails.

The job of the DLBA scheduler is to route/load balance incoming traffic among the DLBA servers in the cluster in a persistent manner. It does this using routing by changing the incoming packet’s MAC address to another machine in the cluster and then forwarding the packet, unchanged, back out through the switch. In this vein, the DLBA scheduler is, essentially, a router.

The scheduler may also simply process the packet itself instead of forwarding it out to another machine in the cluster if the load balancing decision determines that the scheduler machine itself is the best machine to process the connection.

The scheduler machine does not perform the three way handshake with the client, it simply forwards on all incoming packets to itself or another DLBA server in the cluster for processing. Those machines will respond directly back to the client. In this way, all traffic coming into the site comes in through the scheduler and all traffic going out is load balanced among the DLBA servers in the cluster.

Fig. 2 depicts what Pentaflow scheduling looks like physically with a DLBA array 205. The DLBA scheduler is the DLBA server 202 since all incoming traffic to the array 205 comes in through that server.

Referring to Fig. 3, a more logical Pentaflow DLBA array diagram is shown. Fig. 3 shows the same array configuration as Fig. 2, but more clearly shows the relationship of the DLBA scheduler 302 to the other machines in the array 303. The switch 301 sits logically above the array 303. All traffic goes through the DLBA scheduler 302 which routes and load balances traffic throughout the array 303.”

The limitation “assigning a virtual IP address to a scheduler” is clearly supported by the Specification by **at least** the above cited text.

Therefore, the limitations cited in Claims 1 and 16 are fully supported by the specification and comply with 35 U.S.C. § 112, first paragraph. Therefore, Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C. § 112, first paragraph.

IV. FINALITY OF OFFICE ACTION

Applicant believes that the finality of the Office Action is improper. The Office Action has ignored Applicant’s comments regarding the 35 U.S.C. § 112, first paragraph rejection in addition to the actual disclosure of the Specification..

Therefore, Applicant respectfully requests that the Examiner withdraw the finality of the Office Action.

V. CLAIM REJECTIONS – 35 U.S.C. § 103

The Final Office Action rejects Claims 1, 2, 16 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Zisapel-Radware in view of Hasett-PointCast and Bruck-Rainfinity. The rejection is respectfully traversed.

Claims 1 and 16 have been amended to clarify the invention and appear as follows:

1. A process for routing packets through a load balancing array of servers across a network in a computer environment, comprising the steps of:

requesting, by a scheduler, assignment of a virtual IP address to said scheduler, said scheduler is designated as active scheduler for a load balancing array;

wherein all incoming packets from requesting clients destined for the load balancing array are routed through said scheduler via the virtual IP address;

wherein said scheduler routes and load balances a request packet from a requesting client to a load balancing server;

wherein said load balancing server routes and load balances said request packet to a back end Web server;

wherein said back end Web server's response packet to said request packet is sent to said load balancing server; and

wherein said load balancing server sends said response packet directly to said client.

16. (Currently Amended) An apparatus for routing packets through a load balancing array of servers across a network in a computer environment, comprising:

a module for a requesting, by a scheduler, assignment of a virtual IP address to said scheduler, said scheduler is designated as active scheduler for a load balancing array;

wherein all incoming packets from requesting clients destined for the load balancing array are routed through said scheduler via the virtual IP address;

wherein said scheduler routes and load balances a request packet from a requesting client to a load balancing server;

wherein said load balancing server routes and load balances said request packet to a back end Web server;

wherein said back end Web server's response packet to said request packet is sent to said load balancing server; and

wherein said load balancing server sends said response packet directly to said client.

In particular, Zisapel does not teach or disclose a system that requests, by a scheduler, assignment of a virtual IP address to said scheduler, said scheduler is designated as active scheduler for a load balancing array as claimed in Claims 1 and 16. Neither Zisapel nor Hasset nor Bruck mention such a feature and therefore do not contemplate such a system. Bruck teaches away from requesting, by a scheduler, assignment of a virtual IP address to said scheduler, by teaching that one or more of the available virtual IP addresses may be grouped together as a virtual server group (col. 36, lines 36-37).

Therefore, Zisapel in view of Hasset and Bruck does not teach or disclose the invention as claimed.

Claims 1 and 16 are in allowable condition. Claims 2 and 17 are dependent upon independent Claims 1 and 16, respectively. Therefore, Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C. §103(a).

VI. CLAIM REJECTIONS – 35 U.S.C. § 103

The Final Office Action rejects Claims 3, 4, 7, 8, 13, 18, 19, 22, 23, and 28 under 35 U.S.C. § 103(a) as being unpatentable over Zisapel-Radware and Hasett-PointCast and Bruck-Rainfinity in view of “Official Notice”.

The rejection under 35 U.S.C. §103(a) is deemed moot in view of Applicant’s comments regarding Claims 1 and 16, above. Claims 3, 4, 7, 8, 13, and 18, 19, 22, 23, 28, are dependent upon independent Claims 1 and 16, respectively. Therefore, Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C. §103(a).

VII. CLAIM REJECTIONS – 35 U.S.C. § 103

The Final Office Action rejects Claims 5, 6, 14, 15, 20, 21, 29, and 30 under 35 U.S.C. § 103(a) as being unpatentable over Zisapel-Radware and Hasett-PointCast and Bruck-Rainfinity in view of Masters (USPN 6,374,300).

The rejection under 35 U.S.C. §103(a) is deemed moot in view of Applicant’s comments regarding Claims 1 and 16, above. Claims 5, 6, 14, 15, and 20, 21, 29, 30, are dependent upon independent Claims 1 and 16, respectively. Therefore, Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C. §103(a).

VIII. CLAIM REJECTIONS – 35 U.S.C. § 103

The Final Office Action rejects Claims 9-12 and 24-27 under 35 U.S.C. § 103(a) as being unpatentable over Zisapel-Radware and Hasett-PointCast and Bruck-Rainfinity and “Official Notice” in view of Masters (USPN 6,374,300).

The rejection under 35 U.S.C. §103(a) is deemed moot in view of Applicant’s comments regarding Claims 1 and 16, above. Claims 9-12 and 24-27 are dependent upon

independent Claims 1 and 16, respectively. Therefore, Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C. §103(a).

IX. MISCELLANEOUS

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

The Applicants believe that all issues raised in the Office Action have been addressed and that allowance of the pending claims is appropriate. Entry of the amendments herein and further examination on the merits are respectfully requested.

The Examiner is invited to telephone the undersigned at (408) 414-1080 ext. 214 to discuss any issue that may advance prosecution.

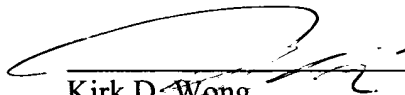
To the extent necessary to make this reply timely filed, the Applicant petitions for an extension of time under 37 C.F.R. § 1.136.

If any applicable fee is missing or insufficient, throughout the pendency of this application, the Commissioner is hereby authorized to any applicable fees and to credit any overpayments to our Deposit Account No. 50-1302.

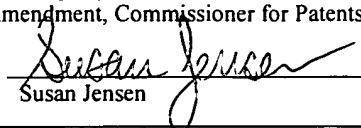
Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.		
on	<u>July 21, 2006</u>	By  Susan Jensen